Single-event latchup modeling based-on coupled physical and electrical transient simulations in cmos technology

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Abstract - **This work presents a SEL modeling based on physical simulations performed by MUSCA SEP3 and electrical simulations. This approach leads to use the layout description and process information (from TCAD, design or ITRS hypotheses) of the CMOS inverter cell to extract the characteristics of the parasitic circuitry. This approach is totally compatible with the Monte Carlo tool, MUSCA SEP3, with the aim to propose estimations of SEL susceptibility as well in terms of cross section, as sensitivity mapping. The latchup transient response is calculated and compared with heavy ion and TPA experimental measurements. The good agreement is shown in terms of latchup current and the electrical steps leading to the SEL occurrence. Complementary comparisons of SEL sensitive area mapping for TPA irradiation is presented and assessed. The ability of the model to take into account the temperature impact on the SEL sensitivity is presented and discussed.**

Index Terms – **Single Event Latchup, circuit model, MUSCA SEP3, temperature impact, CMOS technology**

I. Introduction

Single Event Latchup, (SEL) has been identified on a range of various devices based on CMOS (Complementary Metal Oxide Semiconductor) technology over the last thirty years [1]-[4]. This phenomenon is inherent to the CMOS technology and can be induced by a radiation particle. The charges deposited by the ion modify the electrical field and can trigger the parasitic bipolar structure which leads to the destruction of the device if the supply is not cut off. With technology scaling, reduced nodal capacitances and device sizes decrease the amount of charges induced by radiation necessary to modify the electrical field and create a latchup [5]. Moreover, latchup is known to be temperature dependent [4] [6] [7].

The SEL effect is a reliability challenge for the aerospace industry, and microelectronics manufacturers. Both are focused on the reduction of the SEL sensitivity based on layout and/or process optimization. The modeling of radiation particle induced single event latchup is still a field which is investigated [8][9]. Main works proposed a static modeling of the latchup based on spice models

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without correlate the transient voltage variations and the modification of the electrical field induced by the collection of charges generated by radiation particles.

The aim of this paper is to propose a modeling of the SEL occurrence, induced by a radiation particle, based on coupled physical and electrical simulations and taking into account the device design and the temperature. Some recent works [8][9] proposed a modeling of a transient latchup based on the injection of a transient current, preliminary calculated by TCAD (Technology Computer-Aided Design) simulation, in a spice model. However, this kind of approach has limitations because of long simulation times of TCAD calculations which are antinomic with a Monte-Carlo approach.

In this paper, based on a new methodology using the MUlti SCAles Single Event Phenomena Predictive Platform (MUSCA SEP3) [10] and electrical simulations, the latchup occurrence and characteristics is presented and assessed with heavy ion and TPA (Two Photon Absorption) laser experimental measurements from published work [11] for the 0.18μm technological node.

The second part of this work is focused on the ability of the model to take into account the impact of the temperature on the latchup occurrence. Finally, the SEL sensitivity trends as a function of layout parameters will be proposed and compared to the technological scaling perspective.

II. Modeling of the Single Event Latchup phenomenology

A. Principle of the SEL modeling

The SEL estimation was performed through the MUSCA SEP3 platform, whose the general methodology was presented in previous papers [11] [12]. This platform is based on the modeling of the mechanisms that occur from the strike of a radiation particle into matter to the error occurrence. It can account for every kind of radiation particles: neutrons, protons, heavy ions, muons, and alpha particles. In this work, a new modeling of Single Event Latchup is developed and presented, as shown in Fig. 1.

First, the modeling of the charge diffusion accounts for the ambipolar diffusion mechanisms and recombination processes [13]. Second, the physical modeling of the charges collection accounts for the
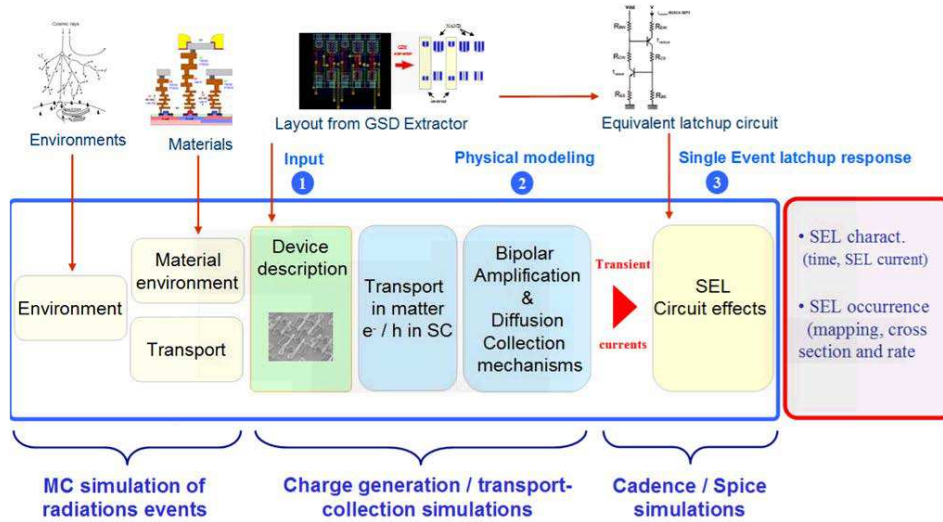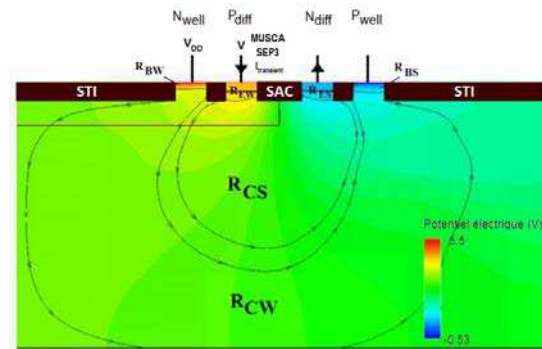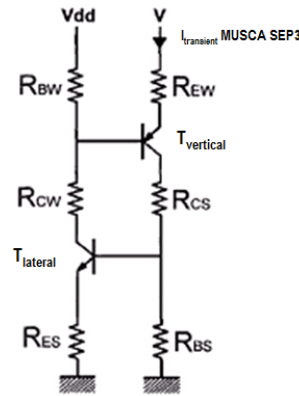
dynamic transport and the multi-charge collection mechanisms, the bias voltage, the layout, the bipolar amplification, the shallow trench isolation (STI) and the fabrication process. The charge collection of each transistor is calculated based on the Front-End Of Line (FEOL) information extracted from the layout (in GDS format). Next, the transient current calculated by MUSCA SEP3 is injected in an equivalent latchup circuit [3] for a transient electrical simulation with the aim to determine the SEL characteristics and occurrence. The electrical transient simulation of the parasitic circuit is performed by the simulator Spectre in the Cadence software.

B. Preliminary TCAD study

A preliminary study by TCAD simulation is performed with the aim to determine the critical areas and the equivalent volumes of silicon which lead to the SEL occurrence in a CMOS inverter. Fig. 2 presents the simulated TCAD structure and the associated parasitic circuitry of the latchup phenomenon [3]. The CMOS inverter analyzed in this section in based on a 0.18µm IBM 7RF bulk CMOS technology [12]. The vertical transistor is a *pnp* transistor which is created by the junctions of the source of the p-MOS transistor (P_{diff} in Fig. 2 (a)), the n-Well and the P-substrate of the inverter. The lateral transistor is a *npn* transistor created by the junctions of the n-Well, the P-substrate and the source of the n-MOS transistor (N_{diff} in Fig. 2 (a)). The current gain of bipolar transistors is related to the base width and the injection efficiency of the emitter-base junction. The base width varies with design rules and the position of the source relative to the Well-Substrate junction. This point is taken into account to calibrate the model cars of the both BJTs (Bipolar Junction Transistor). The values of resistances of the parasitic circuit are

(a)

(b)

Fig. 2 (a) Simplified TCAD structure of 0.18µm CMOS inverter, (b) Equivalent parasitic Latchup circuitry

directly determined from the layout description and taking into account the process (from TCAD data or ITRS hypotheses).

The methodology is based on the determination of the equivalence volumes of silicon which can be deduced by the analysis of the potential lines as presented in Fig. 2 (a). Based on this analysis, the resistance values of the equivalent Latchup circuit (Fig. 2 (b)) are calculated by the following equations:
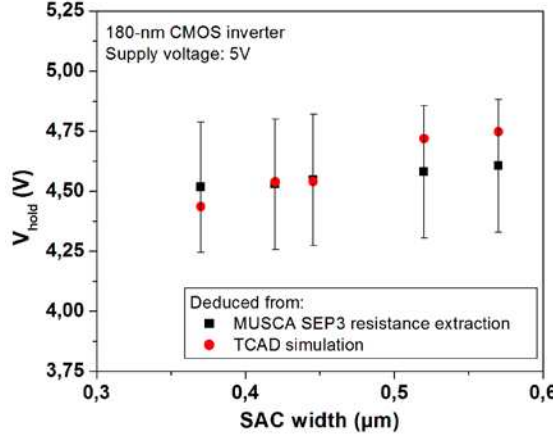
Fig. 3 Comparison of V_{hold} deduced from TCAD simulations (red dots) and deduced from the MUSCA SEP3 resistances extraction (black squares) as a function of the SAC width of the CMOS inverter 0.18μm IBM 7RF.

$$R_{xx} = \rho \frac{l}{A} \qquad (1)$$

$$\rho = \frac{1}{q \times (\mu_n n + \mu_p p)} \qquad (2)$$

Where l and A define the equivalent volumes and ρ and μ correspond to the mean resistivity and mobility of the volume respectively.

The calculation of the resistance values has been validated by TCAD simulations for the specific 0.18μm IBM 7RF bulk CMOS technology as presented in Fig. 3. This validation step has been performed by the comparison of the holding voltage, i.e., V_{hold}, deduced by the resistance calculation and deduced from TCAD Latchup transient current:

$$V_{hold} = V_{trig} - \frac{R_{EW}\left(1 - \frac{R_{ew} R_{ES}}{R_{BS} R_{BW}}\right)}{R_{ES} + R_{CW} + R_{BW}} V_{DD} \qquad (3)$$

$$V_{trig} = V_{DD} - V_{BEth}\left(1 - \frac{R_{EW}}{R_{BS}}\right) \qquad (4)$$

Fig. 3 emphasis the ability of MUSCA SEP3 to extract the relevant value of equivalent resistances which define V_{hold} taking into account the design of the device, i.e., the SAC width. The SAC width is the distance between the p-MOS and the n-MOS transistor of the inverter cell as illustrated in Fig. 2 (a). This design parameter has been presented because of its impact on the SEL robustness of the inverter cell [11]. Actually, a larger SAC increases the spatial isolation of n-MOS and p-MOS transistors which avoids the interaction of the *npn* and *pnp* parasitic bipolar transistors. A good agreement between TCAD and MUSCA SEP3 estimations is presented. The error bars corresponds to the uncertainty of the mean resistivity induced by doping hypothesis of each equivalent resistances. Moreover, the extraction methodology used in MUSCA SEP3 allows for
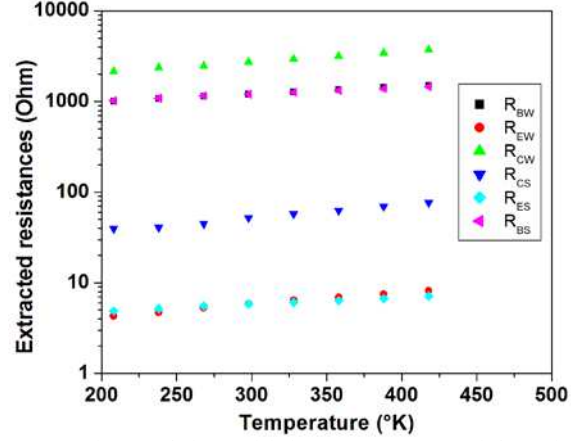

Fig. 4 Evolution of the modeled resistance extracted from the layout of the CMOS inverter 0.18μm IBM 7RF as a function of the room temperature.

taking into account the effects of the temperature which are dominating in the SEL occurrence. Fig. 4 shows the evolution of modeled resistances of the parasitic latchup circuit as a function of the temperature. The range of investigated temperatures is from 208°K to 418°K in order to be representative of usual temperatures of the space environment. As expected, the values of each resistance, i.e., R_{bw}, R_{ew}, R_{cw}, R_{cs}, R_{es}, R_{bs} increase with high temperatures, 50%, 89%, 72%, 97%, 45%, 44% respectively. Actually, an increase in temperature induces an increase in the equivalent resistances (due to a decrease in mobility) of Wells and diffusion regions [13]. The consequences of this temperature dependence on the SEL occurrence are presented in the last section of this work.

C. MUSCA SEP3: Transient latchup results

The aim of Fig. 5 is to show the ability of MUSCA SEP3 coupled to an electrical simulation of the parasitic circuit to model the electrical step leading to the SEL occurrence. The latchup transient current, i.e., P_{diff}, is induced by a heavy ion with a LET of
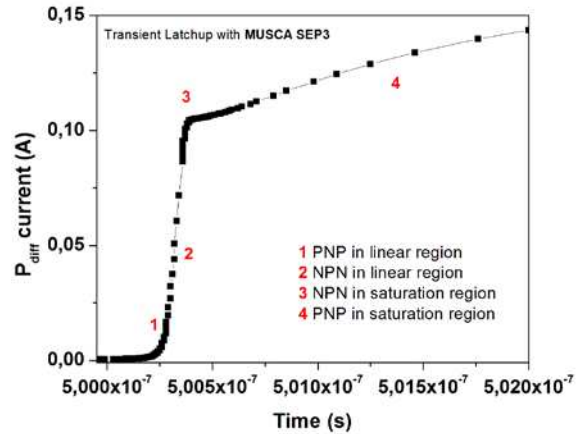

Fig. 5 Transient latchup calculated by MUSCA SEP3 coupled with electrical simulation for a 0.18μm CMOS inverter from IBM at 298°K for a heavy ion with a LET of 21MeV.cm².mg⁻¹

21MeV.cm^2.mg^{-1} in a simplified 0.18μm CMOS inverter from IBM at the room temperature (298°K).

The four transient steps are clearly identifiable and correspond to the well known SEL occurrence process [3]. The transient current $I_{transient}$ injected at the P_{diff} electrode, destabilizes the potential applied to the resistance R_{ew} of the parasitic circuit: (1) the transient current leads to increase the voltage and trig the vertical *pnp* transistor; (2) the current increases and trigs the lateral *npn* transistor; (3) the lateral transistor turns in the saturation region; (4) the vertical *pnp* transistor is locked and the current rises to the reference latchup current. It is important to note that the computing time for the MUSCA SEP3 simulations is lower than 5 seconds for each ion strike. This point is primordial with the aim to propose a SEL prediction (cross-section and cartography) of CMOS devices.

In the next section, the relevance of SEL estimations (cross section and location) is discussed by comparisons with experimental measurements from [11] for the CA18HD 0.18μm technology of Jazz Semiconductor [12].

III. Comparison of SEL occurrence and characteristics: experimental vs. MUSCA SEP3

In this section, the relevance of the SEL estimation calculated by MUSCA SEP3 is assessed by comparisons with experimental heavy ions testing and TPA (Two Photon Absorption) laser SEL sensitivity maps of a SRAM-like test structure in 0.18μm CMOS process from Jazz Semiconductor called CA18HD [12]. The CA18HD process is built on bulk (non-epitaxial) wafers and has six layers of aluminum metallization, shallow trench isolation (STI), dual gate oxides with 57Å (physically measured), and VDD = 1.8V/3.3V. The top metallization consists of 2.8μm thick aluminum metallization with 4.5μm design rule pitch enabling integration of compact high Q inductors. The p-Well resistance is in parallel with the p-Substrate resistance, and therefore reduces the *npn* emitter/base shunting resistance that allows latchup to occur. The p-Substrate doping is 3.10^{15}cm^{-3}. The N- and p-Wells both extend 0.8μm beneath the shallow trench isolation and have a peak doping of 5.10^{17}cm^{-3}. Based on this process description [12] and layout [11] the resistance values of the parasitic circuit are extracted and calculated.

A. Validation of SEL cross section estimations under heavy ion irradiation

Fig. 6 shows the comparison of the experimental SEL cross section presented in [11] and the calculations performed by MUSCA SEP3 for a heavy ion irradiation. The experimental measurements have been done at Lawrence Berkeley National Laboratory with the 10-MeV/u ion beam. The comparison is
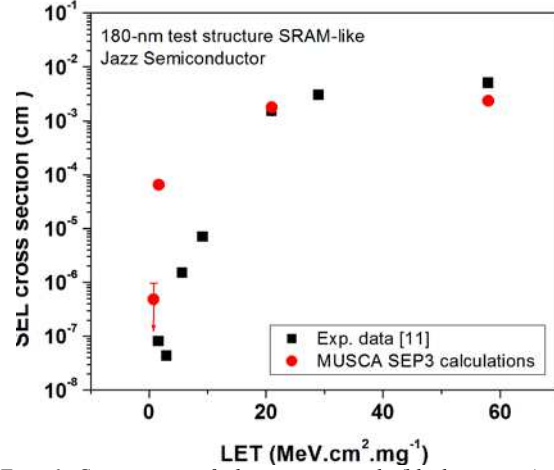

Fig. 6 Comparison of the experimental (black squares) and calculated (red dots) SEL cross section for 0.18μm CMOS SRAM-like test structure for a range of LETs at 298°K with 1.8V bias voltage.

performed for a range of LETs from 1.65MeV.cm^2.mg^{-1} to 58.8Mev.cm^2.mg^{-1}. Fig. 6 reveals a quite good of the calculation and experimental data of the SEL cross section in saturation region (high LETs) are consistent. However, a divergence of the estimation is observed at LET threshold; this divergence can be explained by the limits of the modeling of the bipolar transistors. This point could be improved with a calibration of the BJT model cards using TCAD simulations if the 2D wells and substrate profiles are provided by a semiconductor designer or foundry.

After this quantitative validation of the estimations of the SEL sensitivity with MUSCA SEP, the next section will proposes to identify the SEL critical areas of the device.

B. Analyses of SEL sensitivity area

One of strong interests of the modeling presented in this work is the ability to propose heavy ion SEL-sensitivity maps of a SRAM-like test structure using the 0.18μm technology described previously, for different LETs, as presented in Fig. 7. The layout of n+ and p+ source implants is depicted by pink areas with dark blue edges. The top and bottom pink areas correspond to n-Well and p-Well contacts. Each green dot or red square represents a strike location where the heavy ion is able to trigger SEL, with a LET of 3.5MeV.cm^2.mg^{-1} and 58.8MeV.cm^2.mg^{-1} respectively. For very large LET, i.e., 58.8MeV.cm^2.mg^{-1}, 83% of the inverter cell is susceptible to SEL. Moreover, for lower LET values, the critical area of the inverter can be identified: the drain and the source of the p-MOS transistor are the only sensitive to SEL. This result is consistent with the TPA map from [11], which identifies the n-Well/p-substrate depletion region as the most susceptible
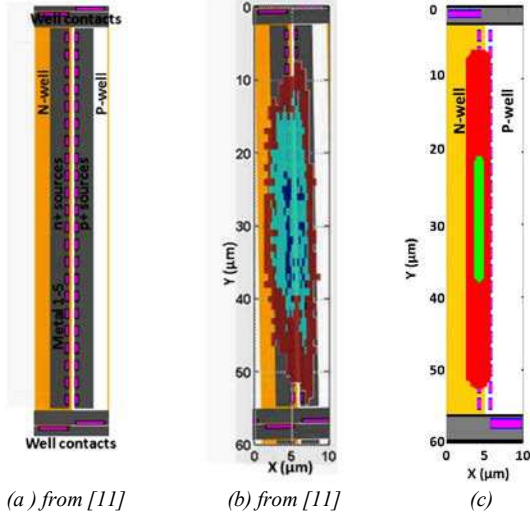
(a) from [11]   *(b) from [11]*   *(c)*

Fig. 7 Comparison of SEL sensitivity map of SRAM-like structure design in 0.18µm technology from Jazz technology: (a) design of the structure presented in [11], (b) experimental TPA SEL sensitivity map from [11] for different laser energy, (c) SEL sensitivity map calculated by MUSCA SEP for a heavy ion with a LET of 58.8MeV.cm^2.mg^{-1} (red area) and 3.5MeV.cm^2.mg^{-1} (green area) at 298°K.

location for triggering the two bipolar transistors. In Fig. 7, it is interesting to note that the cell close to the N-well and P-well contact are immune to SEL due to the maintain of the potential which avoids the trigging of the parasitic bipolar structure. In order to be representative of this edge effect, MUSCA SEP3 avoids the SEL events using the attenuation cell rate deduced from TPA data.

IV. Modeling of the latchup sensitivity dependence to the temperature

In this last section, the impact of the temperature on the latchup sensitivity is modeled and discussed. SEL has been revealed to be temperature dependent [4][6] [7]. High temperatures lead to increase the SEL sensitivity of the device. For this reason, this is essential to take into account the temperature dependence with the aim to propose a relevant and useful SEL estimation. Fig. 8 illustrates the temperature dependence of the transient latchup occurrence in the 0.18µm CMOS inverter. At the room temperature of 208°K (green triangles) the inverter in SEL free, while up to 358°K (black and red symbols) the latchup is trigged and held. Thus, the high temperatures increase the SEL susceptibility of the device which is in good correlation with [4].

Two main reasons can explain this sensitivity trend. First, as presented in Fig. 4, the value of resistances decreases with low temperatures. Thus, the holding voltage is changed. However, if only the effect temperature on silicon resistance is taken into account, V_{hold} will grow that is not in good correlation with the sensitivity trend [4]. For this reason, the impact of
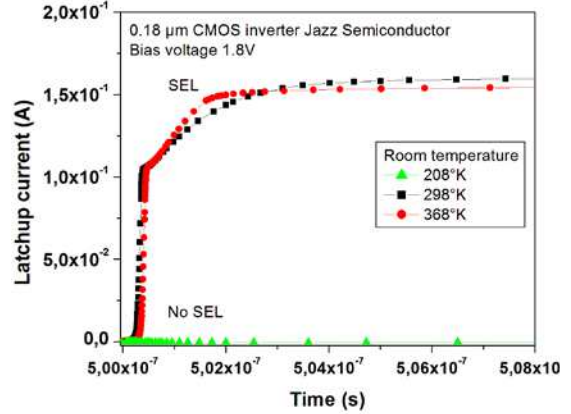

Fig. 8 Transient latchup responses induced by a heavy ion with an LET of 21MeV.cm^2.mg^{-1} for a range of room temperatures from 208°K to 368°K in the 0.18µm CMOS inverter from Jazz Semiconductor biased at 1.8V
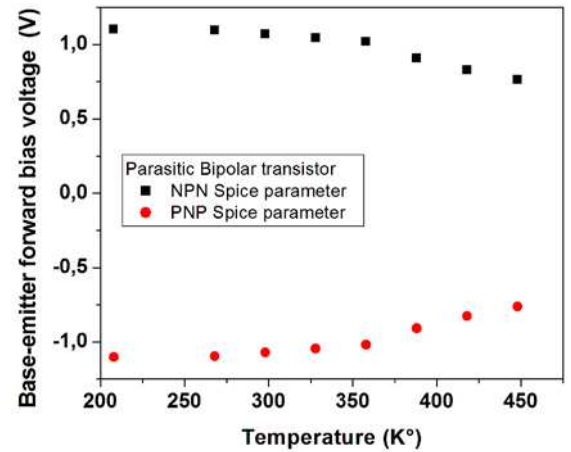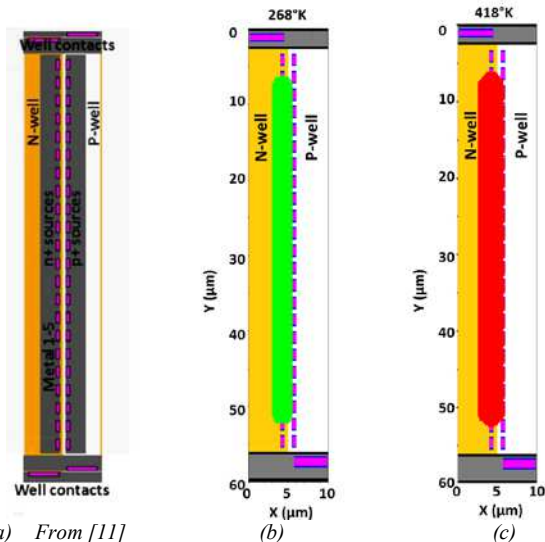

Fig. 9 Evolution of the modeled base-emitter forward bias voltage of the both parasitic bipolar transistor, npn (back squares) and pnp (red dots) of the CMOS inverter 0.18µm as a function of the room temperature ranged from 208°K to 450°K.

temperature on the forward bias voltage of base emitter junction, V_{BEth}, and on the current gain, $β$, of parasitic bipolar transistor must be considered. The current gain of the bipolar transistor increases with the temperature as presented in [16].

An increase in temperature leads to reduce the forward bias voltage of the base-emitter junction, i.e. V_{BEth}, used in equation (4), of the *npn* (back squares) and *pnp* (red dots) parasitic bipolar transistors, as shown in Fig. 9. This decrease in V_{BEth} leads to decrease the potential barrier needed (generated by the collection of charges induced by the heavy ion strike) to trig and hold the parasitic transistors.

As shown in previous section, one of strong interests of the modeling is the ability of MUSCA SEP3 to propose SEL-sensitivity maps. Actually, this point leads to identify critical area and propose some guide line to designers with the aim to improve the design of the logic cells and reduce the latchup occurrence. Fig. 10 presents the SEL sensitivity maps depending on the temperature for a heavy ion with a LET of around

(a) From [11]   (b)   (c)

Fig. 10 Calculated SEL sensitivity map of the 0.18μm simplified CMOS inverter from Jazz technology induced by a heavy ion with a LET of 21MeV.cm^2.mg^{-1} for a temperature of 268°K (b) and 418°K (c) no SEL has been observed at 208°K.

21MeV.cm^2.mg^{-1}.

The simulation are performed for the same 0.18μm simplified CMOS inverter whose the layout is presented in Fig. 10(a). As previously, the layout of n+ and p+ source implants is depicted by pink areas with dark blue edges. The SEL sensitivity area of the device are estimated at 418°K and 268°K, in Fig. 11(b) and Fig.11(c) respectively. The effect of temperature on the sensitive area leads to increase with higher temperatures. An increase in temperature (from 268°K to 418°K) induces an increase in 21% of the sensitive area. It is interesting to note that no SEL has been observed in the calculation at 208°K.

V. Conclusion

This work presents a SEL modeling based on physical simulations performed by MUSCA SEP3 and electrical simulations. This approach leads to use the layout description and process information (from TCAD, design or ITRS hypotheses) of the CMOS inverter cell to extract the characteristics of the parasitic circuitry. This approach leads to propose estimations of SEL susceptibility as well in terms of cross section, as sensitivity mapping. The latchup transient response is calculated and compared with heavy ion and TPA experimental measurements for a 0.18μm technological node.

The good agreement is shown as well in terms of latchup current and the electrical steps leading to the SEL occurrence. Complementary comparisons of heavy ion SEL cross section and sensitivity areas for TPA irradiation are presented and assessed. The ability of the model to take into account the temperature impact on the SEL sensitivity is also presented and discussed.

Based on this work and previous works, the MUSCA SEP3 platform has the ability to propose a deeper estimation to design and semiconductor manufacturers of SEE sensitivity during the development step of a circuitry. The prediction tool leads to anticipate the SEE improvements of penalties as a function of the design as well in terms of soft error, i.e., SET and SEU susceptibility, but also in term of SEL susceptibility.

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